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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,445	11/19/2003	Sandeep Bhatia	CA7035962001	9844
23639 7590 06/08/2007 BINGHAM MCCUTCHEN LLP Three Embarcadero Center San Francisco, CA 94111-4067			EXAMINER TABONE JR, JOHN J	
			ART UNIT 2117	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/718,445

Applicant(s)

BHATIA, SANDEEP

Examiner

John J. Tabone, Jr.

Art Unit

2117

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 November 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-23 are pending in the current application and have been examined. Claims 1, 11 and 21 have been amended.
2. The 35 USC § 112, second paragraph rejections have been withdrawn by the Examiner as a result of Applicant's amendments filed 12/26/2006.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/23/2007 has been entered.

Response to Arguments

4. Applicant's arguments with respect to independent claims 1, 11 and 21 have been considered but are not persuasive. Also, there is a new ground of rejection for claims 21-23 (see 35 USC § 101 rejection).

As per arguments for claims 1, 11 and 21:

The Applicant argues on page 9, second and third paragraphs, “[a]s is generally known in the art and confirmed by Masatake and the Action, a scan chain is a plurality of series connected flip-flops, such as flip-flops 111, 112, ..., 11n. This explicit disclosure by Masatake teaches away from what is claimed by the Applicant in the present claims, because the original clock (CLK) signal of Masatake is not input directly to the flip-flops 111, 112, ..., 11n of the 1st and 2nd scan chains 11, 12. In contrast, the present claims recite that the clock signal is directly input to the first scan chain and the second scan chain during testing. Masatake does not disclose or even suggest this feature of the present claims”.

The Examiner disagrees and asserts that Applicant’s arguments are not persuasive, in fact are defective, because, as disclosed in Applicant’s Figure 3, the clock signal Clock is NOT directly input to Chain-A (i.e. the clock signal is directly input to the second scan chain during testing as recited in claims 1, 11 and 21). Chain-A shows negative-edge triggered flip-flops, that is, the clock signal must go through an inverting stage **before** it clocks the flip-flops of the scan chain. It is generally known in the art and confirmed by Applicant’s own disclosure that a negative-edge triggered flip-flop has an inverter before the clock input of the flip-flop. Masatake also clocks scan chain 11 on the positive edge of CLK (the clock signal is directly input to the first scan chain during testing) and clocks scan chain 12 on the negative edge of CLK via inverter 2. Masatake’s inverter 2 is functionally equivalent to the inverting stage of Applicant’s negative-edge triggered flip-flops in Figure 3. Further, Masatake’s NAND gate 131

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merely passes the clock signal to the respective scan chain "during testing" (i.e. EN is a logic 1, see Drawing 3) and is, therefore, functionally transparent "during testing". The Examiner further asserts that there is no functional difference between Masatake and Applicant's invention of claims 1, 11 and 21 in that **both** clock one scan chain on the positive edge of the clock and **both** clock the second scan chain on the negative edge of the **same** clock, effectively cutting the time it takes to load the scan chains in half. Masatake's Drawing 3 and Applicant's timing diagram of Figure 3 are also equivalent in function.

It is the Examiner's conclusion that independent claims 1, 11 and 21 are not patentably distinct or non-obvious over the prior arts of record namely, Masatake (JP-2003-202362). Therefore, the rejection is maintained. Based on their dependency on independent claims 1, 11 and 21, claims 2-10, 12-20 and 22-23, respectively, stand rejected.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 21-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the

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invention. These claims recite "a computer readable medium storing computer instructions", however, the specification does not disclose any computer readable medium nor suggests/defines which type of medium. In the absence of such a definition, the Examiner is broadly interpreting the computer readable medium in claims 21-23 as a carrier signal as such and, therefore, is non-statutory subject matter. (Also see 35 U.S.C. 101 rejection to follow).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 21-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. These claims recite "a computer readable medium storing computer instructions", however, the specification does not disclose any computer readable medium nor suggests/defines which type of medium. In the absence of such a definition, the Examiner is broadly interpreting the computer readable medium in claims 21-23 as a carrier signal as such and, therefore, is non-statutory subject matter.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

7. Claims 1-5, 11-15 and 21-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Masatake (JP-2003-202362), hereinafter Masatake.

Claims 1, 11 and 21:

Masatake teaches scanning a first test data from an input pin (IN1, Drawing 1) into a first scan chain (Shift Register 11, Drawing 1) during a first state of a clock cycle (T3, Drawing 3) and scanning a second test data from the input pin (IN1, Drawing 1) into a second scan chain (Shift Register 12, Drawing 1) during a second state of the clock cycle (T4, Drawing 3). Masatake also teaches “a clock signal (CLK) of the clock cycle is directly input to the first scan chain and the second scan chain during testing” in claim 1 and 2 where Masatake discloses “Said 1st shift register which operates synchronizing with the 1st edge of **said scanning clock**, said 2nd shift register which operates synchronizing with the 2nd edge of **said scanning clock**” (claim 1) where “said 1st edge being the rising edge and said 2nd edge being a falling edge” (claim 2). (Abstract, ¶s 37, 38, 47, 49, Drawings 1 and 3).

Claims 2, 12 and 22:

Masatake teaches receiving test data from the first scan chain at an output pin (OUT1, Drawing 1) during the first state of the clock cycle (T3, Drawing 3). (Abstract, ¶s 37, 38, 47, 49, Drawings 1 and 3).

Claims 3, 13 and 23:

Masatake teaches receiving test data from the second scan chain at the output pin (OUT2, Drawing 1) during the second state of the clock cycle (T4, Drawing 3). (Abstract, ¶s 37, 38, 47, 49, Drawings 1 and 3).

Claims 4 and 14:

Masatake teaches sending test data from the first and second scan chains (Shift Register 11 and 12, Drawing 1) to a multiplexor (multiplexer 41, Drawing 1), applying a select signal to the multiplexor based on the state of the clock signal (CLK), and causing the multiplexor to output test data from either the first or second scan chain to the output pin based on the select signal (SCO1, Drawings 1 and 3). (Abstract, ¶s 37, 38, 47, 49, Drawings 1 and 3).

Claims 5 and 15:

Masatake teaches scanning the first test data by using a return-to-one clock waveform (T3, T4, T5, Drawing 3) and **using positive edge triggered scan flip-flops** in the first scan chain (Drawing 2). Masatake also teaches scanning the second test data by using the return-to-one clock waveform (T3, T4, T5, Drawing 3) and **using positive edge triggered scan flip-flops** in the second scan chain (Drawing 2). (Abstract, ¶s 37, 38, 47, 49, Drawings 1-3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masatake (JP-2003-202362), hereinafter Masatake.

Claims 8 and 18:

These claims are an obvious alternate representation of claims 5 and 15 and, as such, are rejected as per these rejections. To use a return-to-zero selection criteria instead of return-to-one selection criteria is considered an alternate design choice.

9. Claims 6, 9, 16 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masatake (JP-2003-202362), hereinafter Masatake, in view of Jaramillo et al., (10 Tips for Successful Scan Design: Part two, February 17, 2000, ednmag.com, pp. 77-90), hereinafter Jaramillo.

Claims 6 and 16:

Masatake does not explicitly teach **“associating a lockup register with a beginning flip-flop or an ending flip-flop of the first or second scan chains based on return-to-one selection criteria”**. Jaramillo teaches in an analogous art the general use of using a lockup register with a beginning flip-flop or an ending flip-flop of two separate scan chains. (Fig. 3, page 82). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify Masatake's design of Drawing 1 to include Jaramillo's design suggestions of using lockup latches when interfacing positive and negative edge clock scan flip-flops. The artisan would be motivated to do so because it would prevent Masatake's design of Drawing 1 from shifting data through both edged flip-flops in on clock cycle.

Claims 9 and 19:

These claims are an obvious alternate representation of claims 6 and 16 and, as such, are rejected as per these rejections. To use a return-to-zero selection criteria instead of return-to-one selection criteria is considered an alternate design choice.

10. Claims 7, 10, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masatake (JP-2003-202362), hereinafter Masatake, in view of Jaramillo et al., (10 Tips for Successful Scan Design: Part two, February 17, 2000, ednmag.com, pp. 77-90), hereinafter Jaramillo, in further view of Morton (US 20040078741), hereinafter Morton.

Claims 7 and 17:

Masatake in view of Jaramillo does not explicitly teach "associating a negative edge triggered scan-in lockup register with the beginning flip-flop of the first scan chain if the beginning flip-flop of the first scan chain has a positive edge trigger", "associating a positive edge triggered scan-in lockup register with the beginning flip-flop of the second scan chain if the beginning flip-flop of the second scan chain has a negative edge trigger" and "associating a negative edge triggered scan-out lockup register if the

ending flip-flop of the second scan chain has a negative edge trigger". However, Masatake in view of Jaramillo does teaches the general use of using a lockup register with a beginning flip-flop or an ending flip-flop of two separate scan chains to prevent a shoot-through condition. (Fig. 3, page 82). Morton teaches in an analogous art "associating a negative edge triggered scan-in lockup register with the beginning flip-flop of the first scan chain if the beginning flip-flop of the first scan chain has a positive edge trigger". (Fig. 2, ¶ 21). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify lockup latch configuration of Masatake in view of Jaramillo with Morton's design of Fig. 2. The artisan would be motivated to do so because it would enable the lockup latch configuration of Masatake in view of Jaramillo to present input data IN1 of Drawing 1 to the input of scan chain 11 on the inactive portion of the clock, thus preventing shoot-through. Also, the claim limitations "associating a positive edge triggered scan-in lockup register with the beginning flip-flop of the second scan chain if the beginning flip-flop of the second scan chain has a negative edge trigger" and "associating a negative edge triggered scan-out lockup register if the ending flip-flop of the second scan chain has a negative edge trigger" are obvious design choices given the above mentioned modification to Masatake in view of Jaramillo.

Claims 10 and 20:

These claims are an obvious alternate representation of claims 7 and 17 and, as such, are rejected as per these rejections. To use a *positive edge* triggered scan-in lockup register with a *negative edge* trigger beginning flip-flop of the first scan chain

instead of a *negative edge* triggered scan-in lockup register with a *positive edge* trigger beginning flip-flop of the first scan chain is considered an alternate design choice.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


GUY LAMARRE
PRIMARY EXAMINER

 6/5/07
John J. Tabone, Jr.